

logic of data(binary)  
D8,7,8,5,4,3,2,1,0

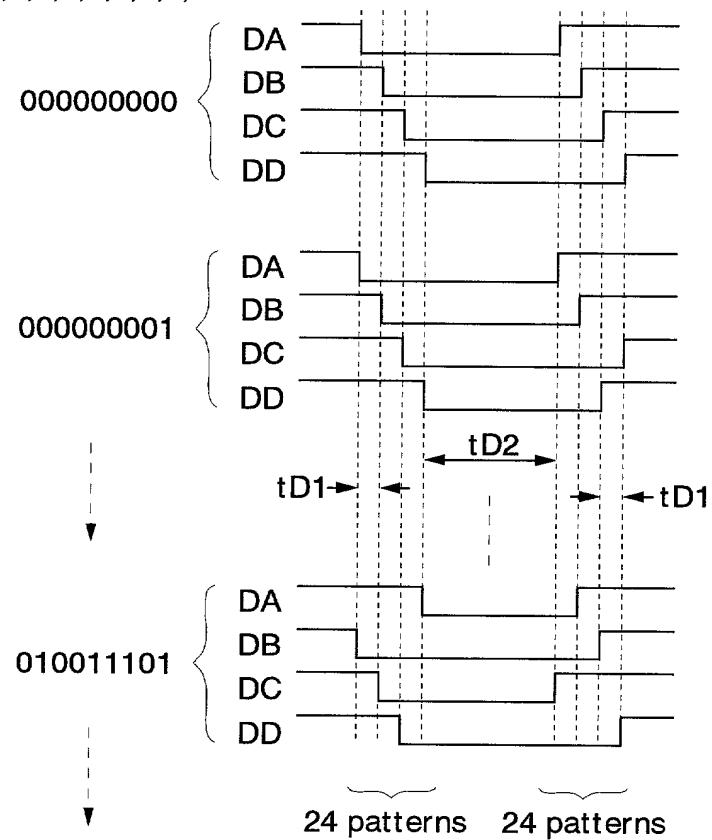
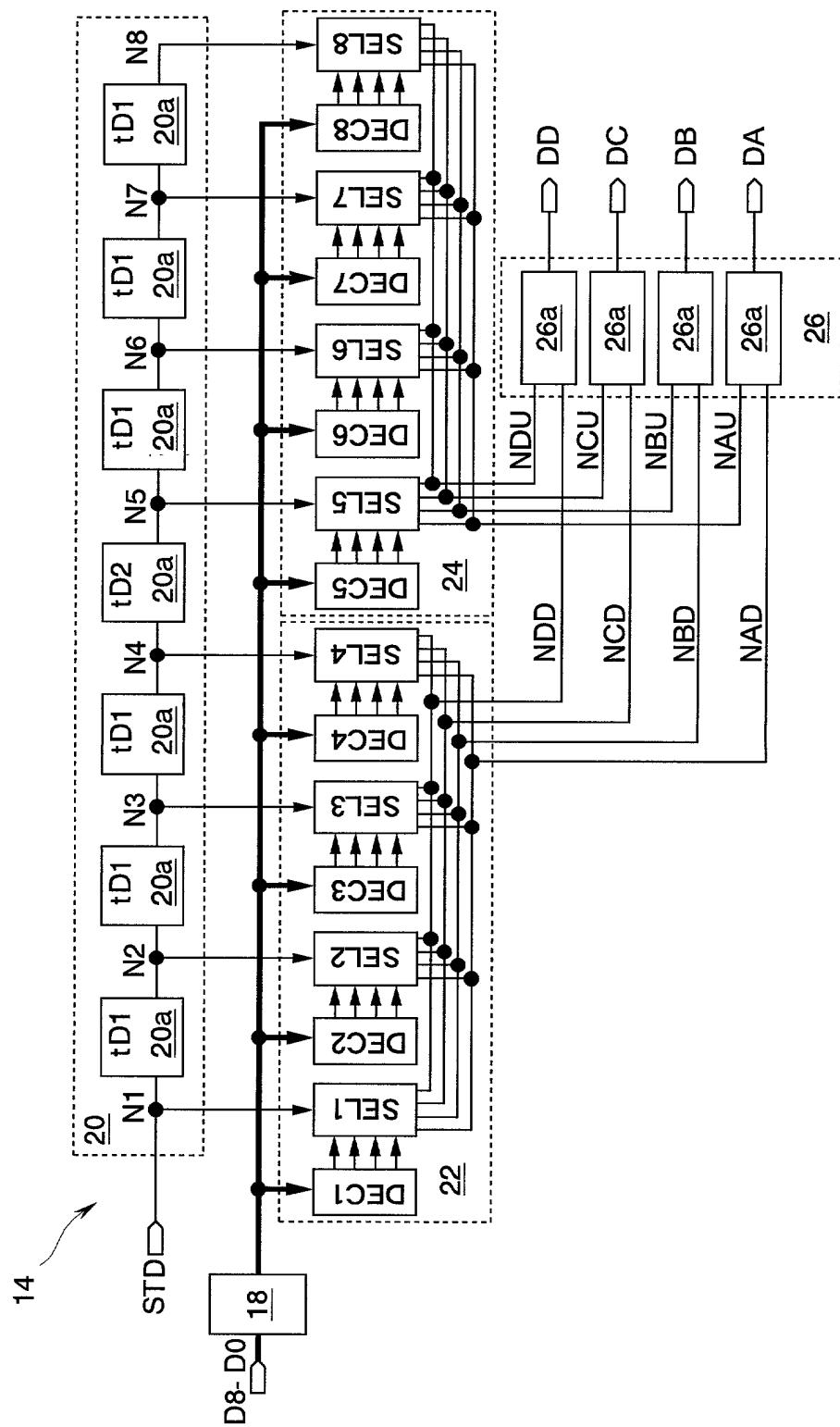


Fig. 1

Fig. 2



18

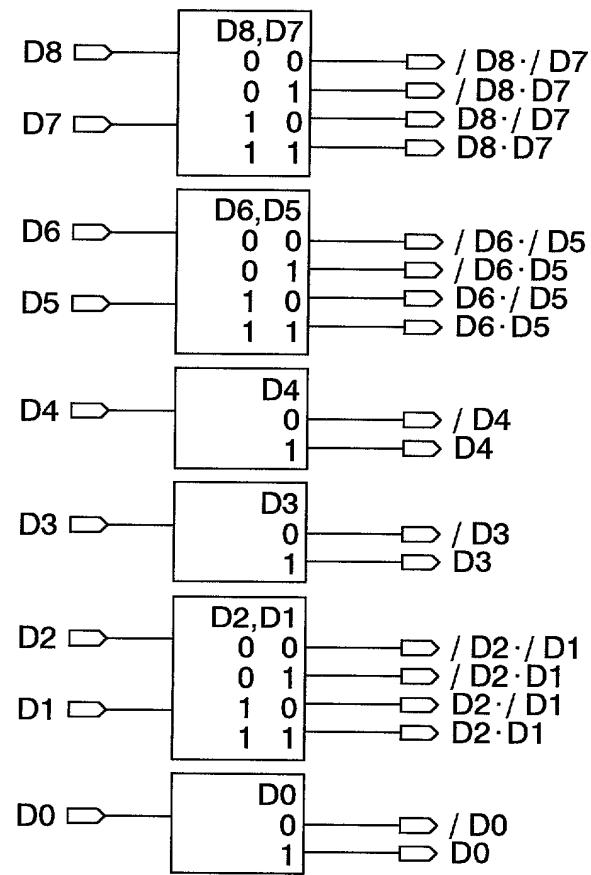


Fig. 3

No.	order of edges	logic L1				logic L2				logic L3			
		D8,7	D6,5	D4	D3	D8,7	D6,5	D4	D3	D8,7	D6,5	D4	D3
0	ABCD	00	00	0	0	11	00	00	00	11bar	00	00	00
1	ABDC	00	00	1	0	11	00	1	0	11bar	00	00	1
2	ACBD	00	01	0	0	11	01	0	0	11bar	0	01	0
3	ACDB	00	01	1	0	11	01	1	0	11bar	0	01	1
4	ADBC	00	10	0	0	11	10	1	0	11bar	0	10	0
5	ADCB	00	10	1	0	11	10	1	0	11bar	0	10	1
6	BACD	00	11	0	0	11	11	0	0	11bar	0	11	0
7	BADC	00	11	1	0	11	11	1	0	11bar	0	11	1
8	BCAD	01	00	0	0	11	00	0	1	11bar	1	00	0
9	BCDA	01	00	1	0	11	00	1	1	11bar	1	00	1
10	BDAC	01	01	0	1	01	01	0	1	11bar	1	01	0
11	BDCA	01	01	1	1	01	01	1	1	11bar	1	01	1
12	CABD	01	10	0	0	11	10	0	1	11bar	1	10	0
13	CADB	01	10	1	0	11	10	1	1	11bar	1	10	1
14	CBAD	01	11	0	0	11	11	0	1	11bar	1	11	0
15	CBDA	01	11	1	1	11	11	1	1	11bar	1	11	1
16	CDAB	10	00	0	0	11	-	-	-	11	-	00	0
17	CDBA	10	00	1	0	11	-	-	-	11	-	00	0
18	DABC	10	01	0	0	11	-	-	-	11	-	01	0
19	DACB	10	01	1	0	11	-	-	-	11	-	01	1
20	DBAC	10	10	0	0	11	-	-	-	11	-	10	0
21	DBCA	10	10	1	1	11	-	-	-	11	-	10	1
22	DCAB	10	11	0	0	11	-	-	-	11	-	11	0
23	DCBA	10	11	1	1	11	-	-	-	11	-	11	1

for leading edge

for trailing edge

Fig. 4

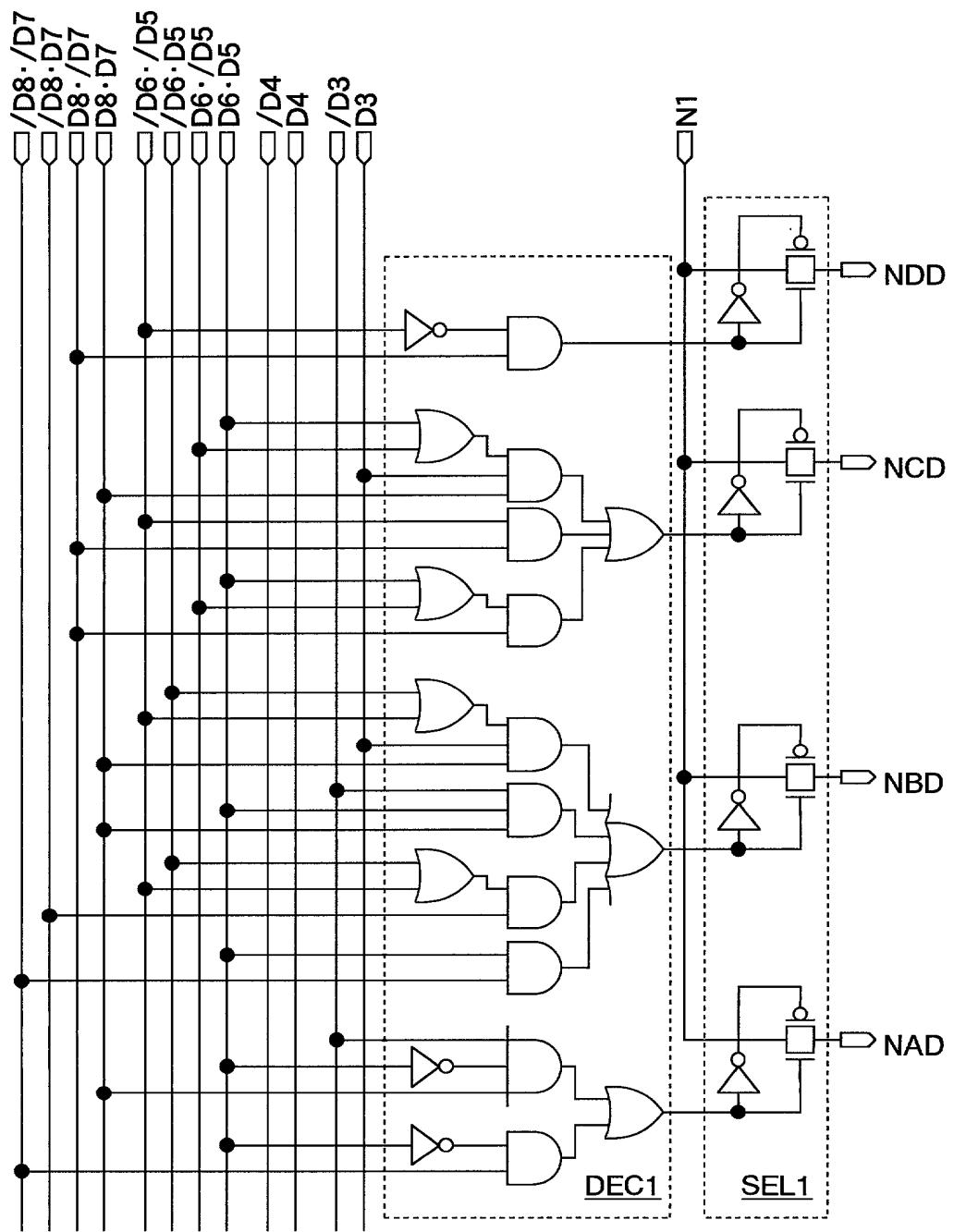


Fig. 5

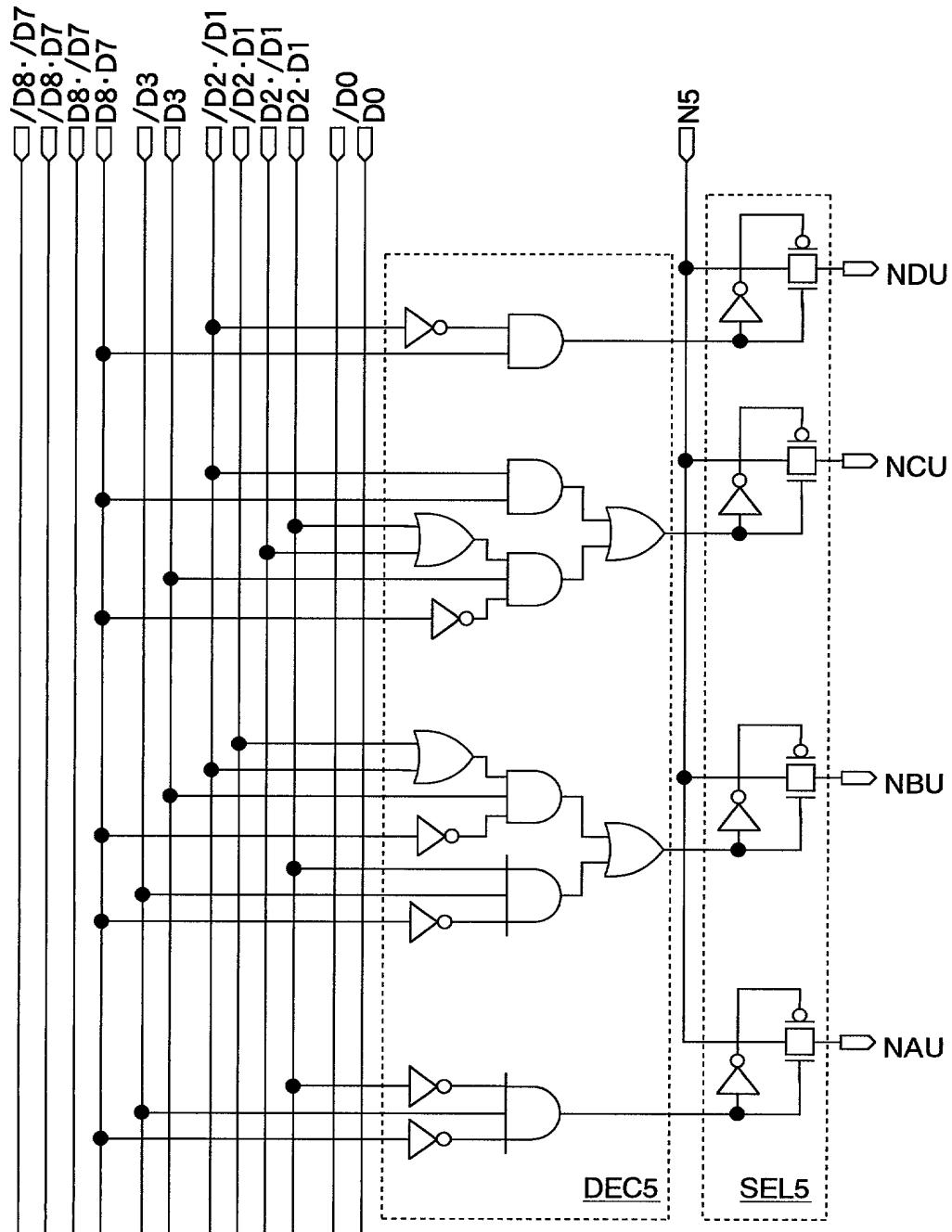


Fig. 6

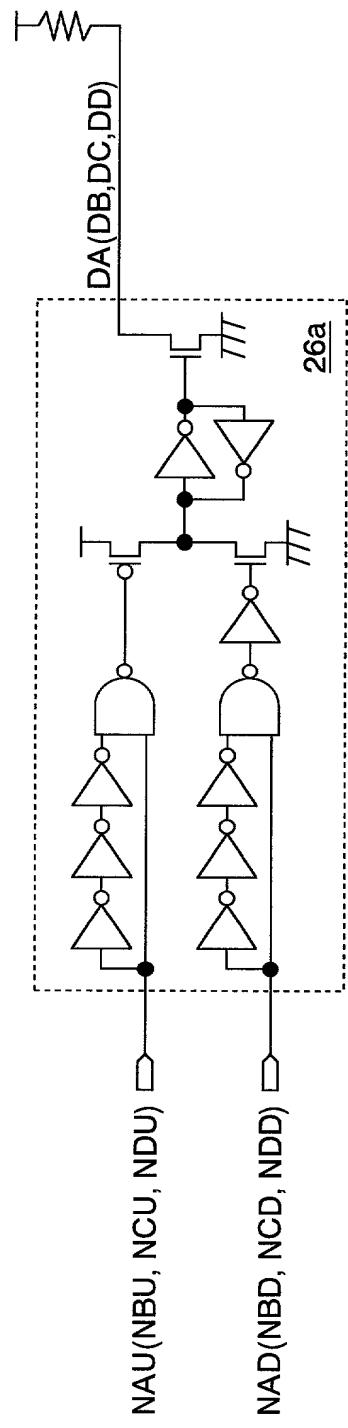


Fig. 7

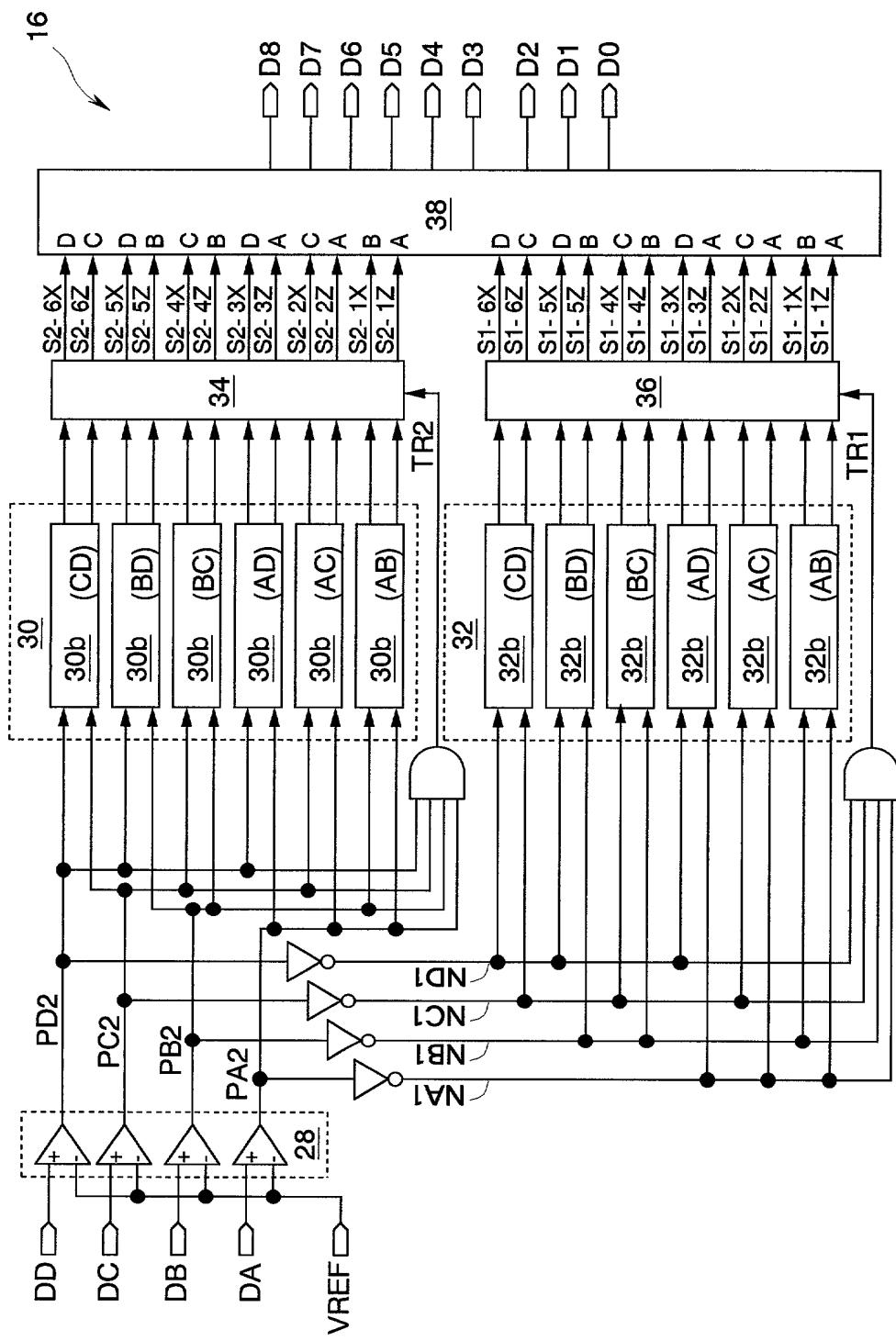


Fig. 8

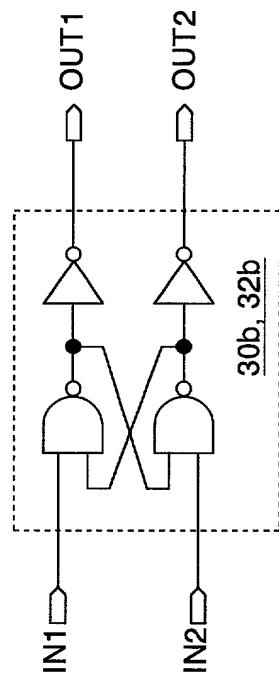


Fig. 9

No.	order of edges	output OUT of comparator 32b						output OUT of comparator 30b						for trailing edge							
		D8,7	D6,5	D4	D8,7	D6,5	D4	D3	1,2,3,4,5,6	D8,7	D3	D2,1	D0	Logic L1	Logic L2	Logic L1	Logic L2	Logic L1	Logic L2		
0	ABCD	111111	00	0	11	00	0	0	111111	11bar	0	00	0	1111110	11bar	0	00	1	0		
1	ABDC	111110	00	1	11	00	1	0	111110	11bar	0	00	1	111011	11bar	0	01	0	0		
2	ACBD	111011	00	0	11	01	0	0	111011	11bar	0	01	0	111001	11bar	0	01	1	1		
3	ACDB	111001	00	0	11	01	1	0	111001	11bar	0	01	1	111100	11bar	0	10	0	0		
4	ADBC	111100	00	0	11	10	0	0	111100	11bar	0	10	0	111000	11bar	0	10	1	0		
5	ADCB	111000	00	1	11	10	1	0	111000	11bar	0	11	0	011111	11bar	0	11	0	1		
6	BACD	011111	00	0	11	01	0	0	011111	011111	0	01	0	011110	11bar	0	11	1	1		
7	BADC	011110	00	0	11	11	1	0	011110	11bar	0	11	1	011110	11bar	0	11	0	0		
8	BCAD	001111	01	00	0	11	00	0	1	001111	11bar	1	00	0	001111	11bar	1	00	1	0	
9	BCDA	000111	01	00	1	11	00	1	1	000111	11bar	1	00	1	000111	11bar	1	00	1	0	
10	BDAC	010110	01	01	0	11	01	0	1	010110	11bar	1	01	0	010110	11bar	1	01	0	0	
11	BDCA	000110	01	01	1	11	01	1	1	000110	11bar	1	01	1	000110	11bar	1	01	1	1	
12	CABD	101011	01	10	0	11	10	0	1	101011	11bar	1	10	0	101011	11bar	1	10	0	0	
13	CADB	101001	01	10	1	11	10	1	1	101001	11bar	1	10	1	101001	11bar	1	10	1	0	
14	CBAD	001011	01	11	0	11	11	0	1	001011	11bar	1	11	0	001011	11bar	1	11	0	0	
15	CBDA	000011	01	11	1	11	11	1	1	000011	11bar	1	11	1	000011	11bar	1	11	1	1	
16	CDAB	100001	10	00	0	11	10	0	1	100001	11	-	00	0	100001	11	-	00	0	0	
17	CDBA	000001	10	00	1	000001	11	-	00	1	110100	11	-	01	0	110100	11	-	01	0	0
18	DABC	110100	10	01	0	110100	11	-	01	0	110000	11	-	01	1	110000	11	-	01	1	0
19	DACB	110000	10	01	1	110000	11	-	01	1	010100	11	-	10	1	010100	11	-	10	1	0
20	DBAC	010100	10	10	0	010100	11	-	01	0	000100	11	-	10	1	000100	11	-	10	1	0
21	DBCA	000100	10	10	1	000100	11	-	01	1	100000	11	-	11	0	100000	11	-	11	0	0
22	DCAB	100000	10	11	0	100000	11	-	01	1	000000	11	-	11	1	000000	11	-	11	1	1
23	DCBA	000000	10	11	1	000000	11	-	01	1	000000	11	-	11	1	000000	11	-	11	1	1

Fig. 10

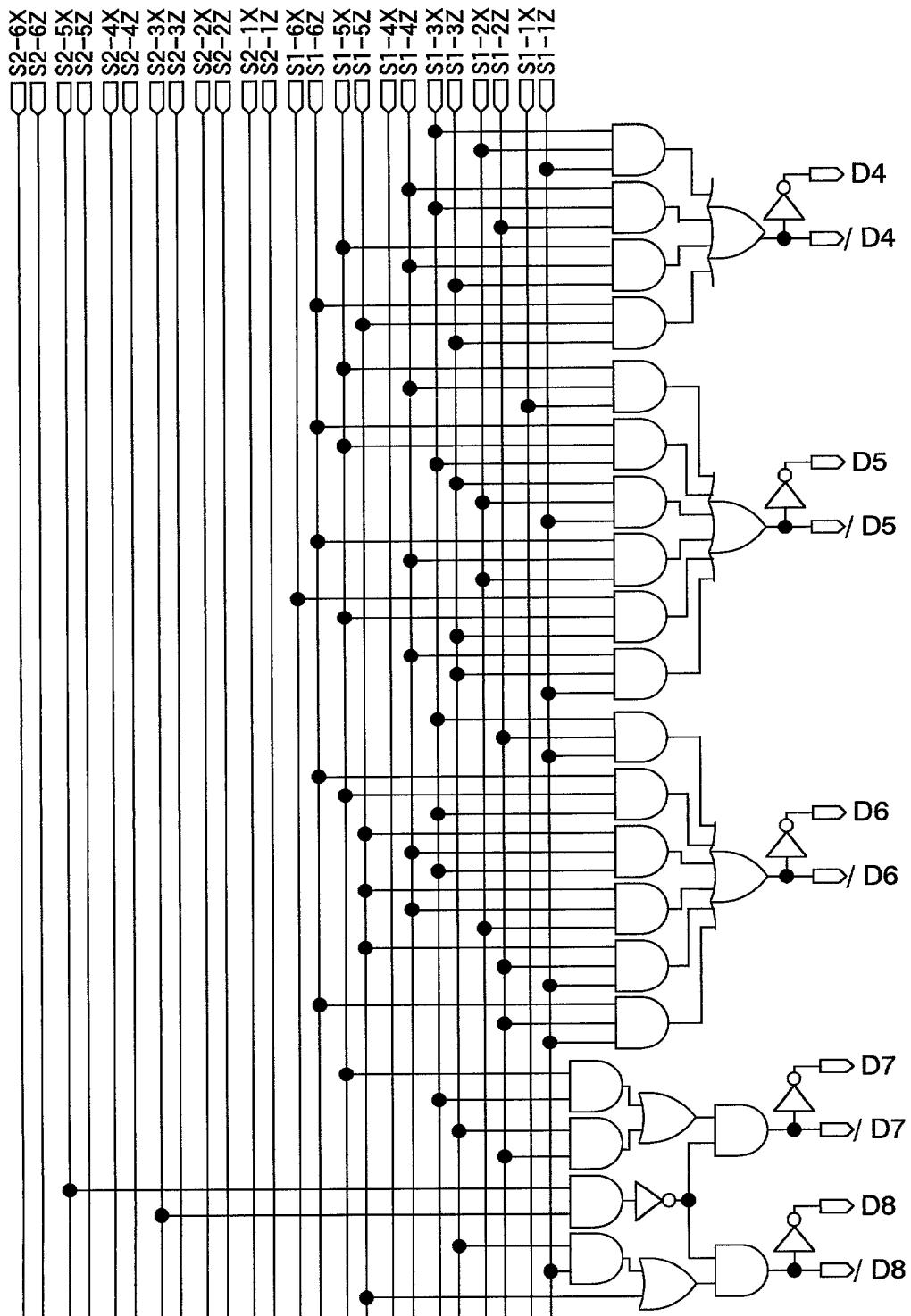


Fig. 11

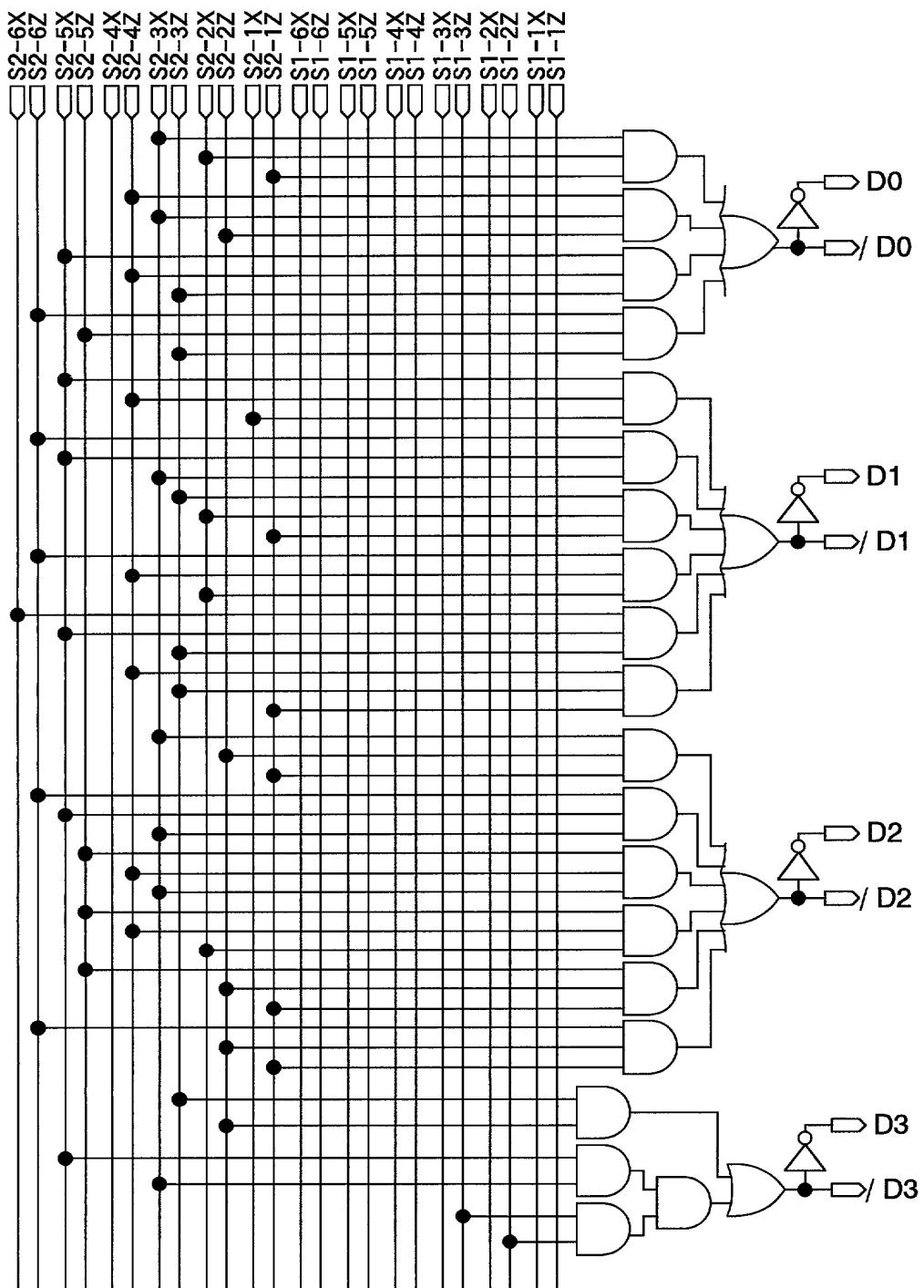
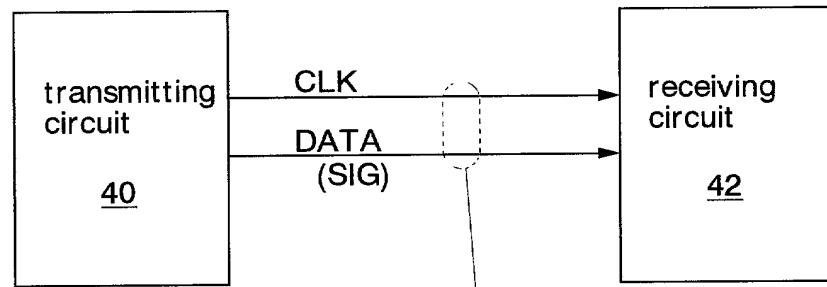


Fig. 12



logic of data(binary)  
DT1,0

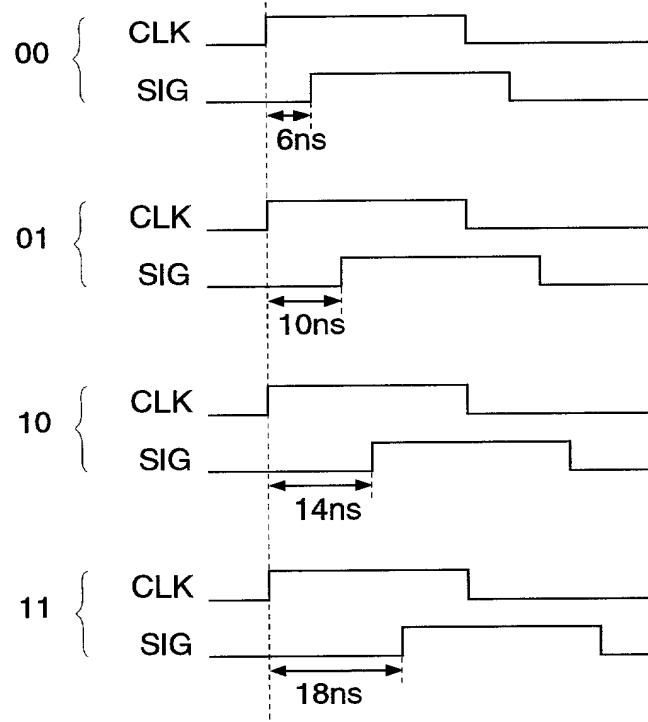


Fig. 13

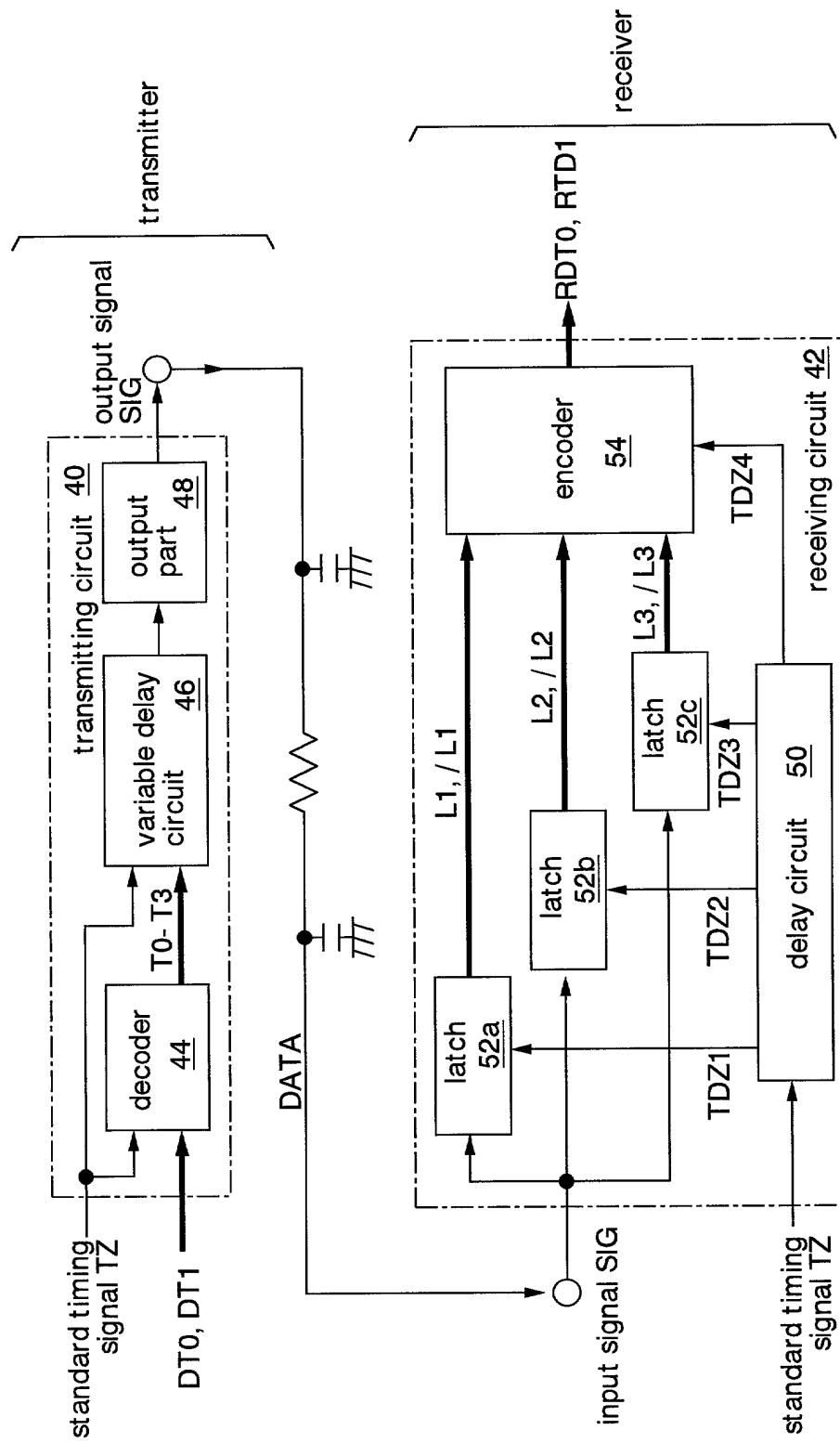
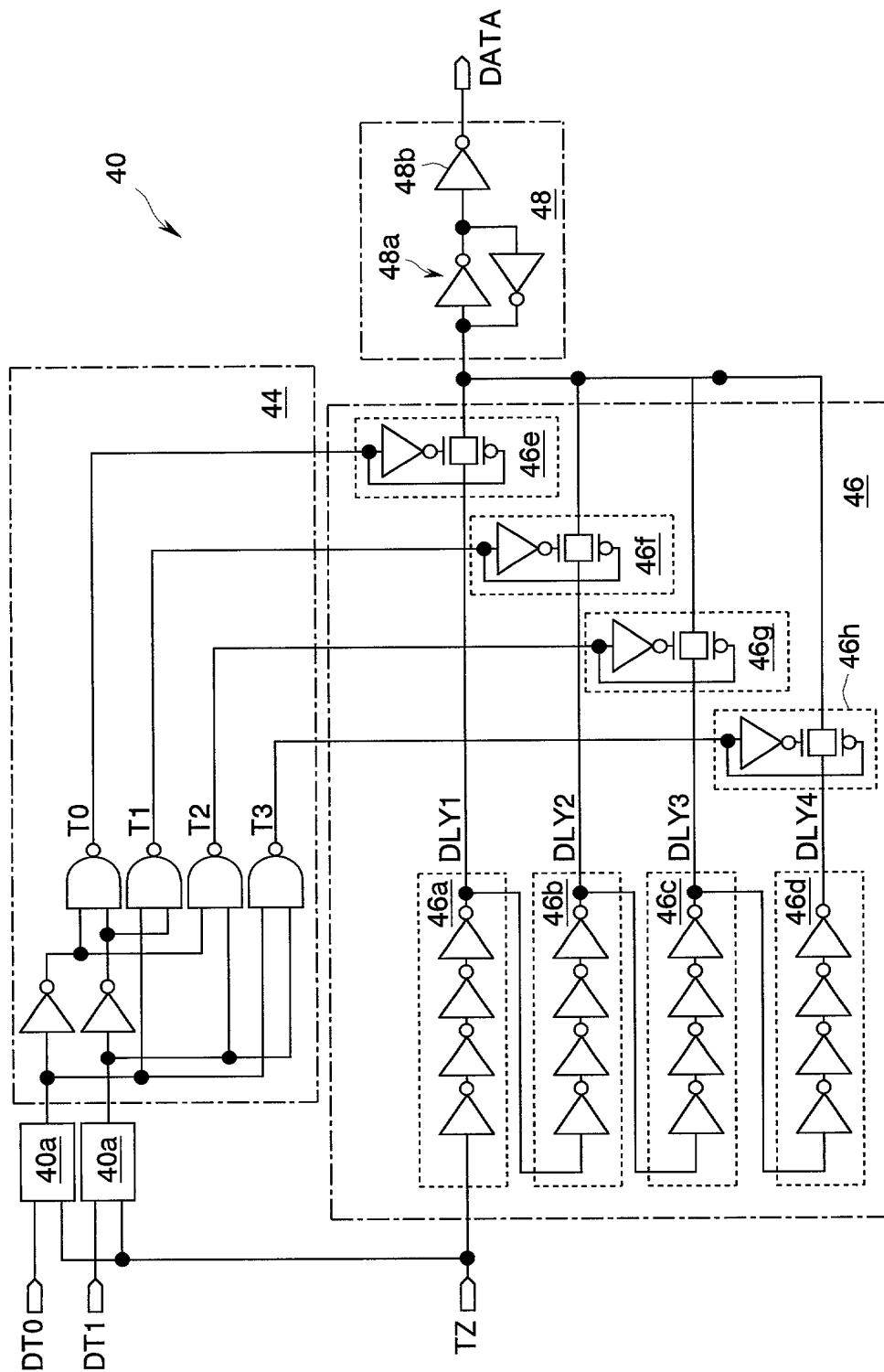


Fig. 14

Fig. 15



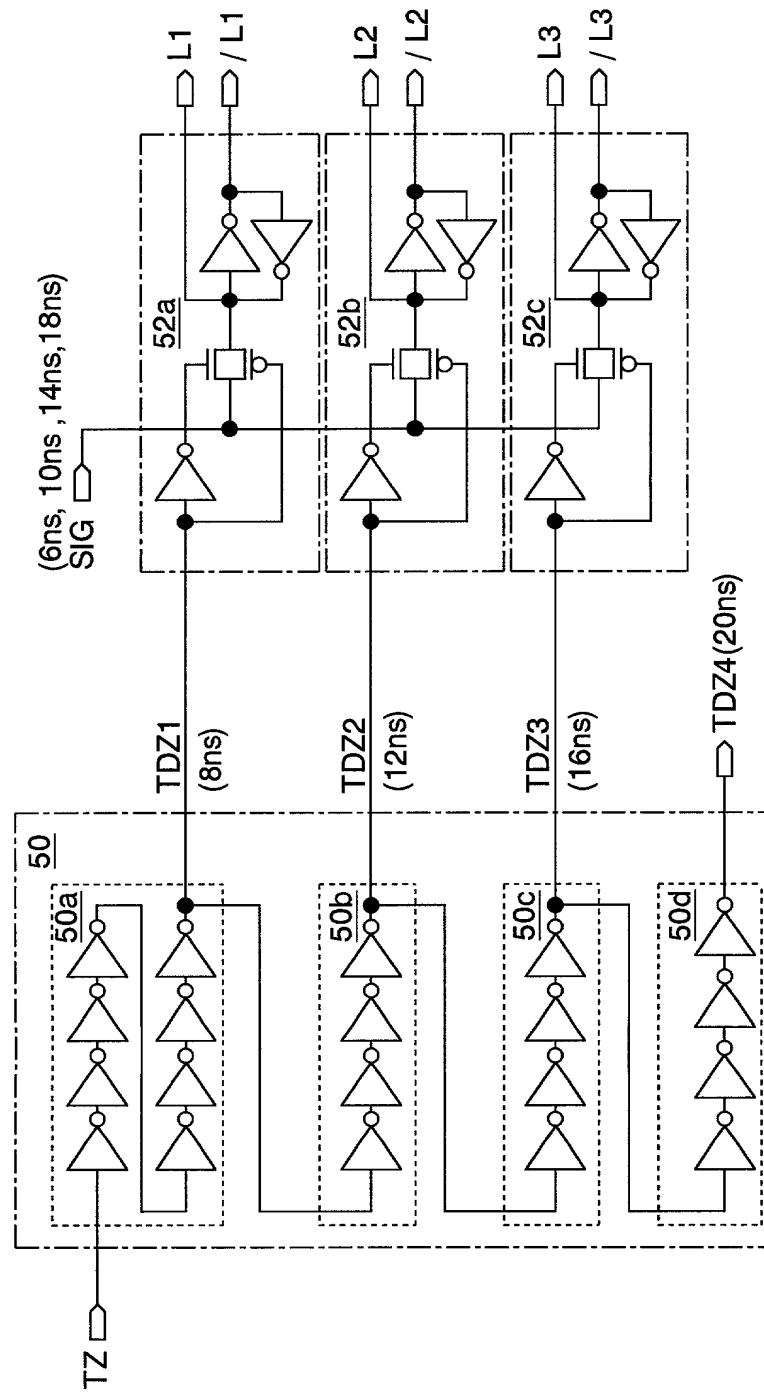


Fig. 16

Fig. 17

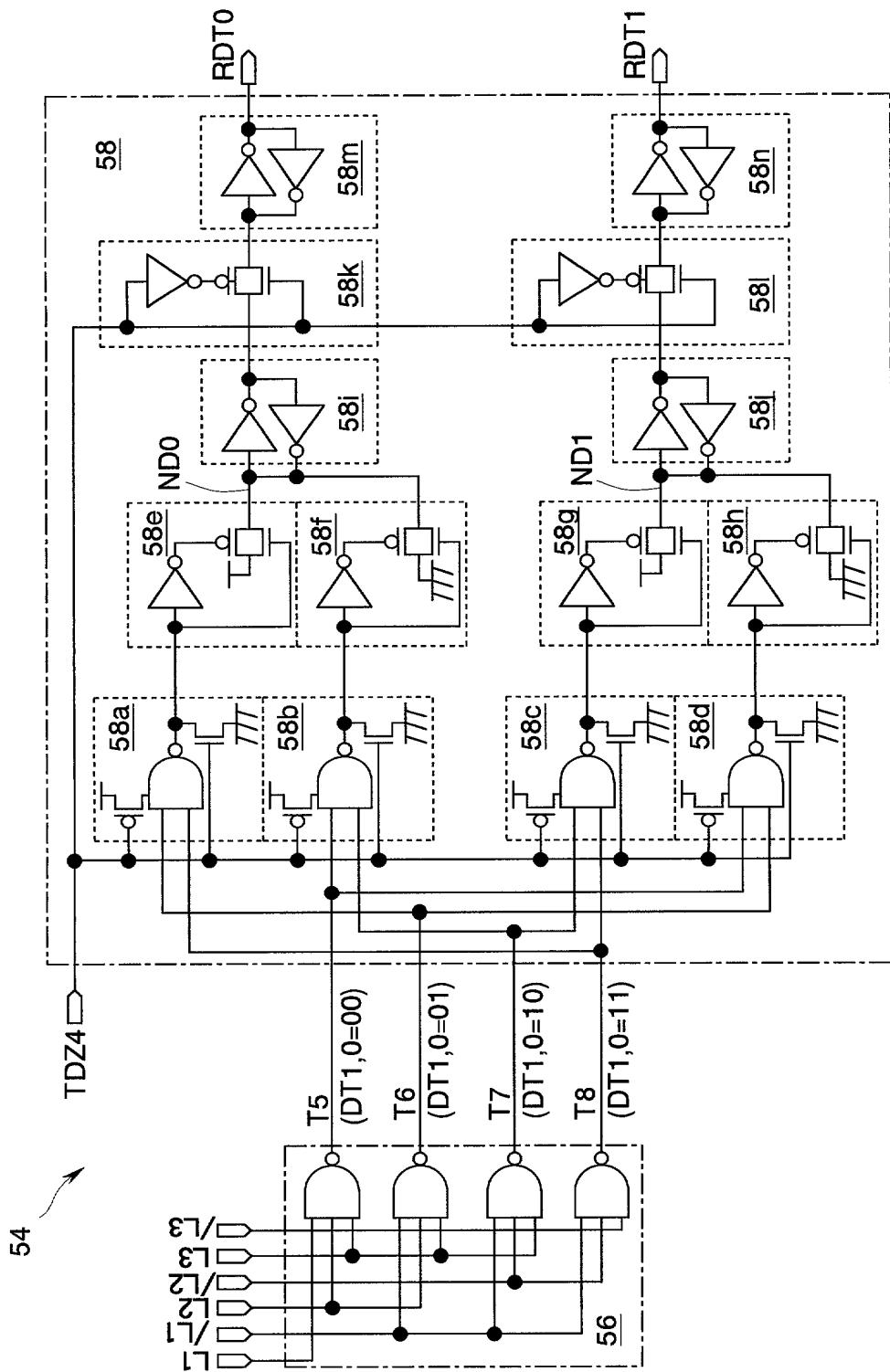
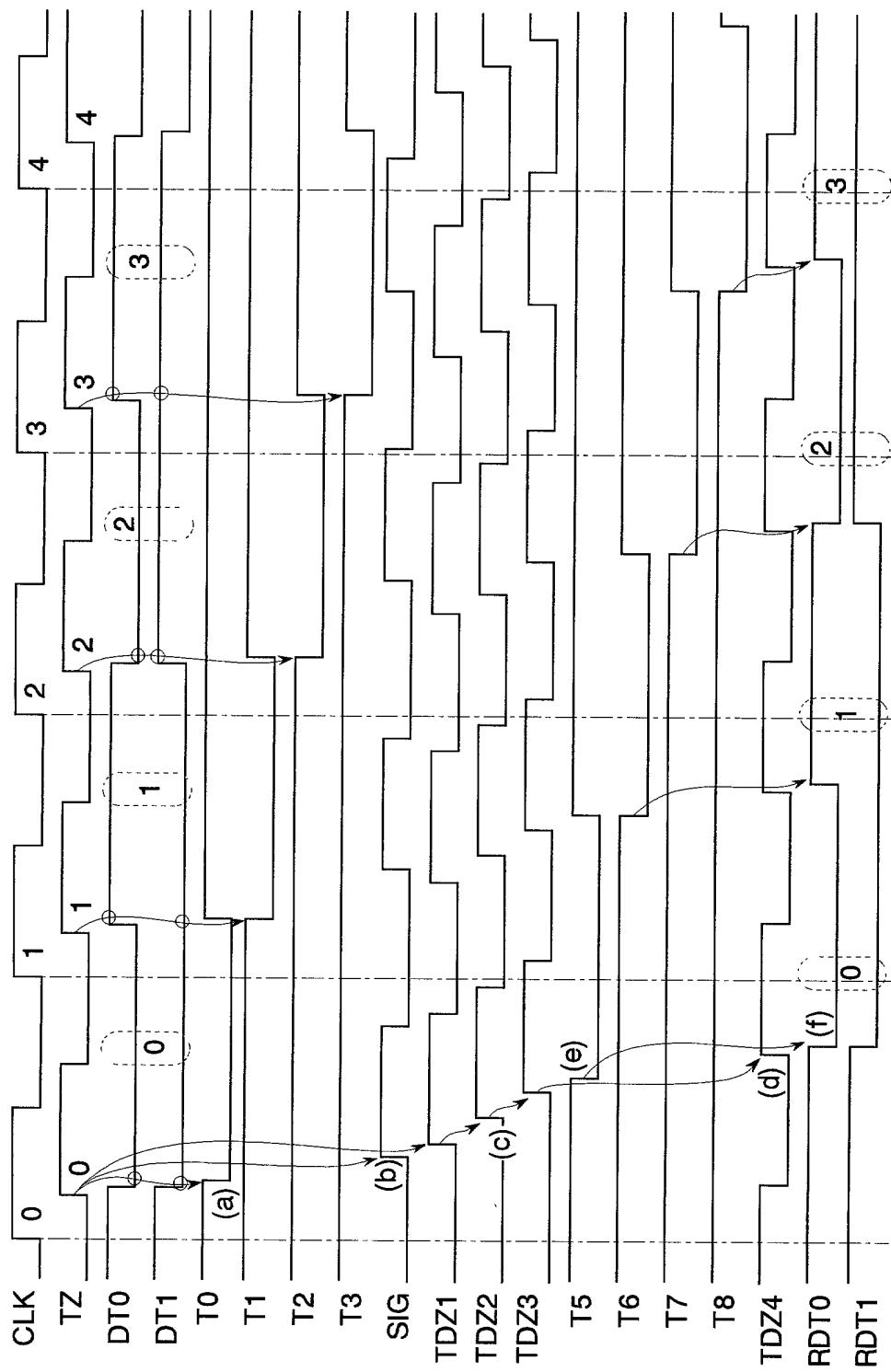


Fig. 18



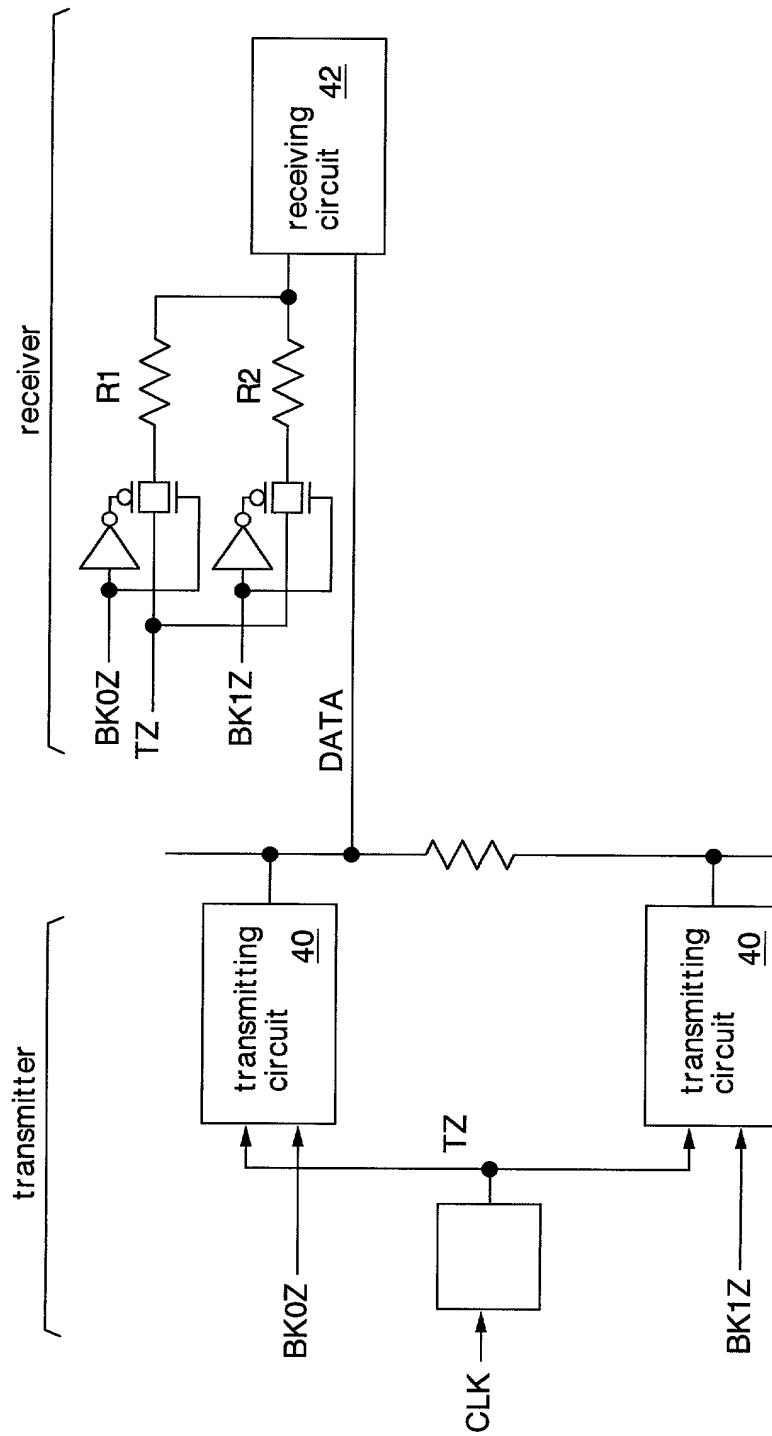


Fig. 19

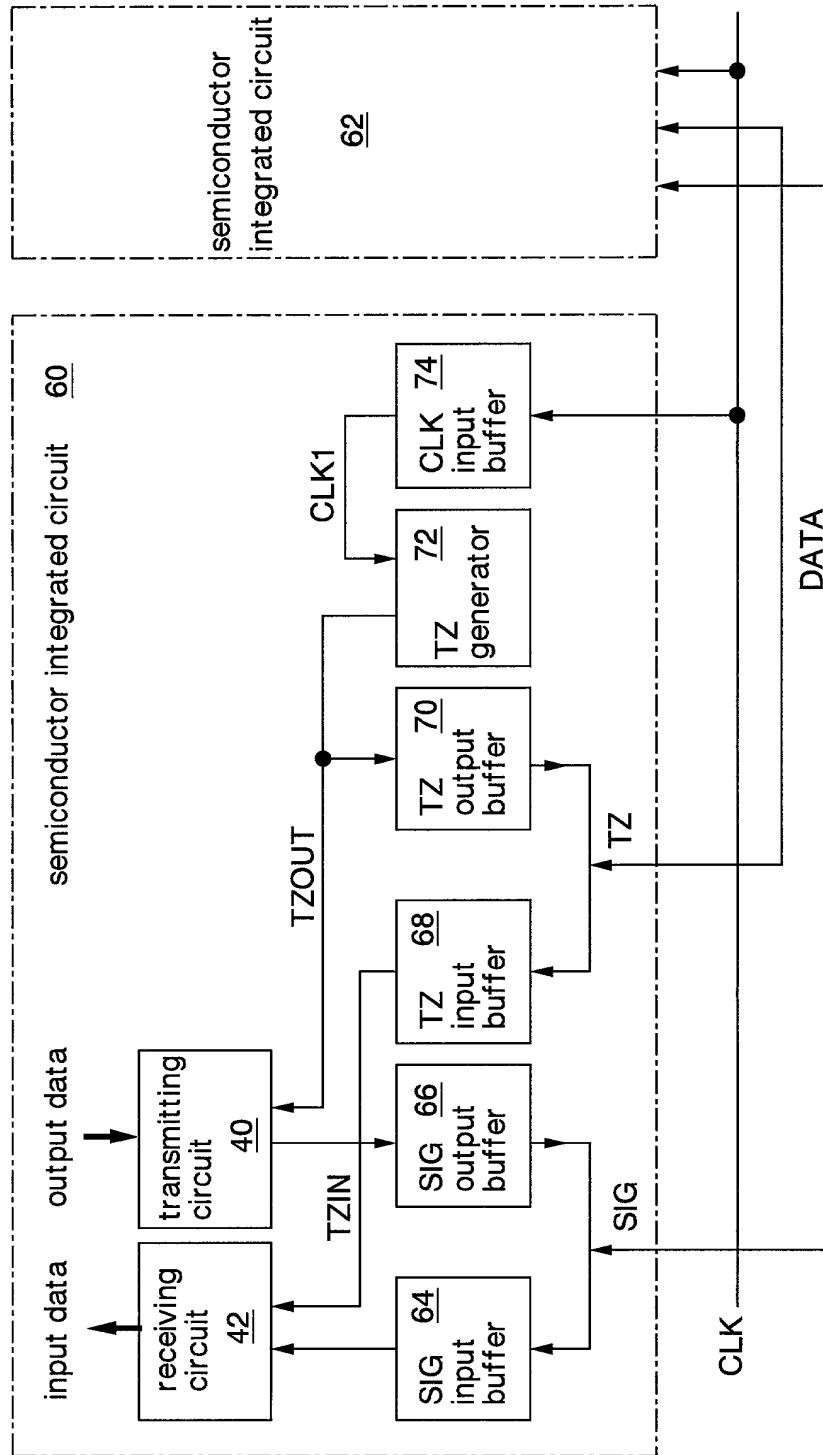


Fig. 20

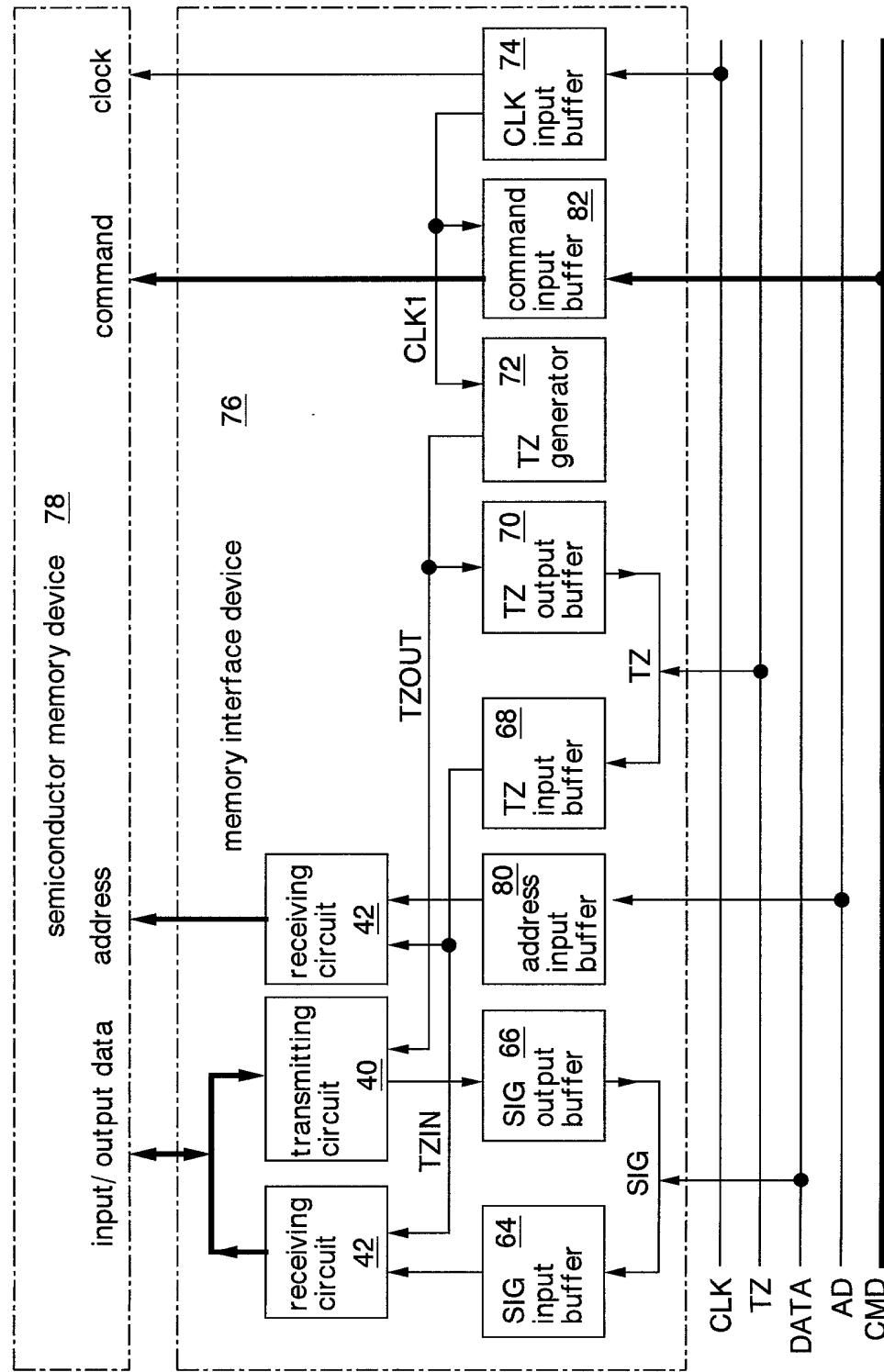


Fig. 21